

2025 中国研究生创“芯”大赛 · EDA 精英挑战赛

一、赛题名称

基于 AI 的跨工艺模拟集成电路行为建模

二、命题单位

香港应用科技研究院有限公司

三、赛题背景

在全球集成电路（IC）产业持续高速发展的驱动下，模拟集成电路作为片上系统（SOC）的核心功能单元，其重要性日益显著。当前模拟集成电路设计面临的一个主要问题是如何复用现有的 IP 来实现在新工艺节点的敏捷设计，从而缩短产品上市时间（time to the market）。这不仅是一个市场需要，也是一个技术挑战。正是基于这个市场需要和技术挑战，我们提出了这样的一个竞赛试题-基于 AI 的跨工艺模拟集成电路行为建模。实现模拟集成电路的跨工艺自动化设计实际包括两个层次的电路 IP 迁移，即电路原理图的自动迁移（re-sizing）和物理版图的自动迁移。考虑到问题的复杂性以及竞赛时间限制，该试题将只涉及与电路原理图的自动化迁移（re-sizing）相关的跨工艺电路建模问题。

当前机器学习技术，如深度神经网络（DNN）、高斯过程回归（GPR）、支持向量机（SVM）等算法，凭借其强大的数据驱动建模能力，为跨工艺节点建模研究开辟了全新路径，基于历史工艺数据构建预测模型的研究已成为领域内的热点方向。精准的跨工艺节点建模能够帮助设计团队在新工艺导入阶段提前完成电路性能评估，有效缩短设计验证周期。然而，当前研究仍面临瓶颈：当目标工艺数据稀缺时，如何有效

利用源工艺的大规模数据提升模型的泛化能力，这一问题亟待学术界与工业界协同突破。

四、赛题描述

本赛题聚焦跨工艺节点的模拟电路的预测问题，要求参赛者开发创新的算法，例如机器学习，迁移学习，大语言模型（LLM）等人工智能（AI）算法，或任何其他算法。训练数据包含大量 A 工艺与少量 B 工艺的电路仿真数据，其涵盖不同种类的运算放大器拓扑结构，例如两级运算放大器和 5T 运算放大器等。隐藏的测试数据为大量 B 工艺的电路仿真数据。出题方将提供完整的训练数据集和电路拓扑结构，参赛者基于此来设计其模型，最终模型将在隐藏的测试集上接受准确性和泛化性的严格检验。

4.1 问题：

在这个问题中，参赛者需要利用所提供的信息（包含大量原有工艺 A 和少量目标工艺 B 的仿真数据）创建跨工艺电路模型，并利用模型预测两种运算放大器的性能指标(图 1)，和放大器的设计参数反推（图 4）。

A. 5T 运算放大器性能预测模型

该模型的输入是基于目标工艺 B 的 **5T 运算放大器**（图 2）电路设计参数，如器件物理尺寸和偏置电流，输出是针对目标工艺 B 预测的 **5T 运算放大器** 的性能指标，如运放的增益、单位增益带宽、相位裕度、共模抑制比和压摆率等。

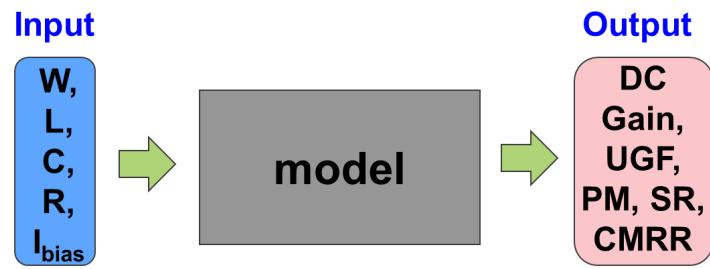


图 1: 运算放大器性能预测模型

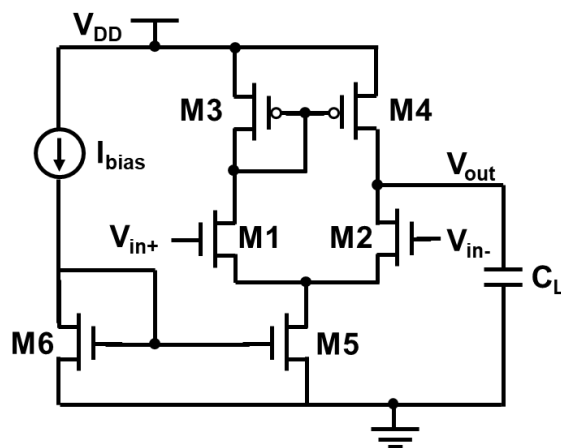


图 2: 5T 运算放大器的电路拓扑结构

电路设计参数	单位	电路性能指标	单位
w1	um	增益 (Gain)	X
w2	um	相位裕度 (PM)	°
w3	um	单位增益带宽 (UGF)	Hz
l1	um	共模抑制比 (CMRR)	X
l2	um	压摆率 (SR)	V/s
l3	um		
I _{bias}	A		

表 1: 5T 运算放大器的电路设计参数和电路性能指标

B. 两级运算放大器性能预测模型

该模型的输入是基于目标工艺 B 的两级运算放大器 (图 3) 设计参数, 如器件物理尺寸, 补偿电阻, 补偿电容和偏置电流, 输出是针对目标工艺 B 预测的两级运算放大器的性能指标, 如运放的增益、单位增益带宽、相位裕度、共模抑制比和压摆率等。

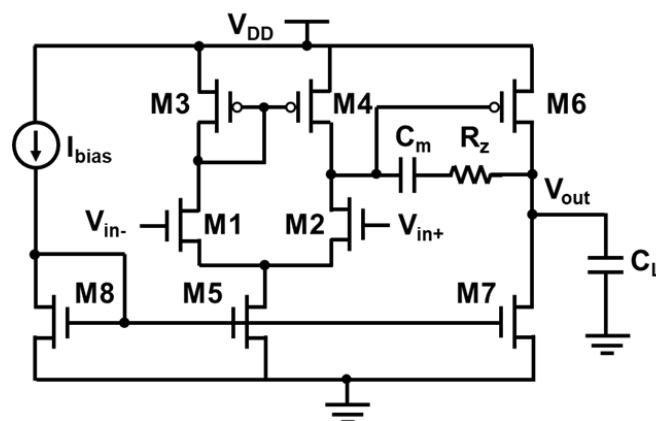


图 3: 两级运算放大器的电路拓扑结构

电路设计参数	单位	电路设计参数	单位	电路性能指标	单位
w1	um	l1	um	增益 (Gain)	X
w2	um	l2	um	相位裕度 (PM)	°
w3	um	l3	um	单位增益带宽 (UGF)	Hz
w4	um	l4	um	共模抑制比 (CMRR)	X
w5	um	l5	um	压摆率 (SR)	V/s
Cm	F	I _{bias}	A		
Rz	ohm				

表 2: 两级运算放大器的电路设计参数和电路性能指标

C. 5T 运算放大器参数反推模型

该模型的输入是基于目标工艺 B 的 **5T 运算放大器** 的性能指标，如运放的增益、单位增益带宽、相位裕度、共模抑制比和压摆率等，输出是针对目标工艺 B 预测的 **5T 运算放大器** 的设计参数，如晶体管物理尺寸和偏置电流，要求模型需实现跨工艺场景下的参数精准反推。

D. 两级运算放大器参数反推模型

该模型的输入是基于目标工艺 B **两级运算放大器** 电路的性能指标，如运放的增益、单位增益带宽、相位裕度、共模抑制比和压摆率等，输出是针对目标工艺 B 预测的 **两级运算放大器** 电路设计参数，例如器件物理尺寸，补偿电阻，补偿电容和偏置电

流，要求模型需实现跨工艺场景下的参数精准反推。

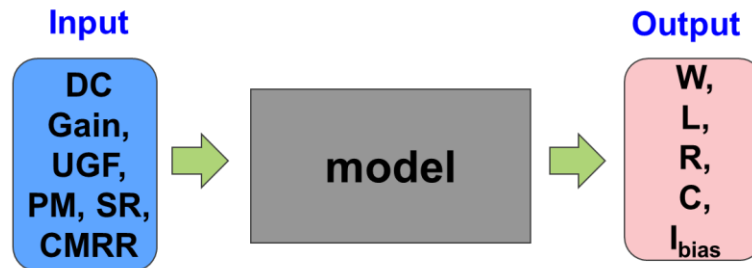


图 4：运算放大器参数反推模型

4.2 提交说明

赛题最终提交内容包含两个部分：

1. **原工程项目代码**：提交可执行的算法代码，需要以 Python 为接口，确保代码结构清晰、注释完整，具备良好的可复现性。
2. **设计报告**：以 Word 格式提交队伍作品简介，内容需涵盖算法设计方案、详细的实验测试效果分析以及全面的实验总结，要求逻辑清晰、论述详实。

五、评分标准

总分 100 分，A, B, C, D 四个部分各占 25 分。参赛者提交的程序将针对 **5T 运算放大器**和**两级运算放大器**两类电路进行测试。评分将综合考查预测准确性、模型泛化能力等维度，依据综合表现进行排名，按名次确定最终得分。

每题的评分规则如下：

1. **预测准确性（20%）**：将模型在训练数据集中的目标工艺 B 下的训练数据上进行测试，通过计算预测结果与训练数据的误差，例如均方误差（**MSE**）、平均绝对误差（**MAE**）和决定系数（**R²**）等指标，评估模型预测的精准度。出题方将会根据这三个指标来计算模型优值（**FoM**）给模型打分，并对所有参赛队进行排名，

排名越高得分越高。

2. 模型泛化能力（80%）：考察模型在隐藏的测试数据集下的稳定性与适应性，分析模型对稀缺目标工艺数据的处理能力。出题方将会通过计算预测结果与测试数据的误差，例如均方误差（MSE）、平均绝对误差（MAE）和决定系数（R²）等指标，来对模型的泛化能力进行分数，并对所有参赛队进行排名，排名越高得分越高。具体的打分规则如下(Detailed scoring methodology):

在 **A** 和 **B** 部分中对电路的第 i 个指标(或者反推的设计参数)计算其优值(FoM_i):

$$FoM_i = 0.3 \times MSE_{nom} + 0.3 \times MAE_{nom} + 0.4 \times R^2_{norm} \quad (1)$$

$$MSE_{nom} = 1 - \min(MSE / MSE_{worst}, 1) \quad (2)$$

$$MAE_{nom} = 1 - \min(MAE / MAE_{worst}, 1) \quad (3)$$

$$R^2_{norm} = \max(R^2, 0) \quad (4)$$

其中 MSE_{worst} 为所有参数队中在第 i 个电路指标（或者反推的设计参数）最差的 MSE ， MAE_{worst} 为所有参数队中在第 i 个电路指标最差的 MAE 。

这个电路的总的优值 FoM 为(The total FoM is):

$$FoM = \sum (FoM_i) \quad (5)$$

然后各队在 **A** 与 **B** 部分根据这个 FoM , 即方程(5)进行排名, 第一名得 100%的这部分的模型准确性和泛化能力得分, 第二名得 90%的这部分得分, 第三名得 80%的这部分的得分。从第四名开始以后的名次依次递减 5%的这部分得分, 直到第十名递减到 45%的这部分得分。从第十一名开始以后的名次依次递减 3%的这部分得分,

一直递减到第 25 名得 0% 的这部分得分。

在 C 和 D 部分中对电路的反推的设计参数计算其优值 (FoM)

$$FoM = 0.5 \times MSE'_{nom} + 0.5 \times MAE'_{nom} \quad (6)$$

$$MSE'_{nom} = 1 - \min(MSE' / MSE'_{worst}, 1) \quad (7)$$

$$MAE'_{nom} = 1 - \min(MAE' / MAE'_{worst}, 1) \quad (8)$$

$$MSE' = \frac{1}{n} \sum_{i=1}^n \sum_{k=1}^k \left(\frac{y_k - y_k'}{y_k} \right)^2 \quad (9)$$

$$MAE' = \frac{1}{n} \sum_{i=1}^n \sum_{k=1}^k \left| \frac{y_k - y_k'}{y_k} \right| \quad (10)$$

其中 MSE'_{worst} 为所有参数队中在反推的设计参数上最差的 MSE' ， MAE'_{worst} 为所有参数队中在反推的设计参数上最差的 MAE' 。 y_k 为真实的第 k 个设计参数向量， y_k' 为预测的第 k 个设计参数， n 为样本数量。

然后各队在 C 与 D 部分根据方程(6)进行排名。

最后根据各队在 A, B, C 和 D 这四个部分的得分总和来确定最终的排名。

以 A 部分的泛化分数为例，其中 A 部分的泛化分数满分为 $25 \times 80\% = 20$ 分，下面显示在 A 部分的前 30 名次的参赛队在该部分的泛化分数得分表：

名次	A 部分相对泛化得分 [%]	A 部分绝对泛化得分
1	100%	20
2	90%	18
3	80%	16

4	75%	15
5	70%	14
6	65%	13
7	60%	12
8	55%	11
9	50%	10
10	45%	9
11	42%	8.4
12	39%	7.8
13	36%	7.2
14	33%	6.6
15	30%	6
16	27%	5.4
17	24%	4.8
18	21%	4.2
19	18%	3.6
20	15%	3
21	12%	2.4
22	9%	1.8
23	6%	1.2
24	3%	0.6
25	0%	0
26	0%	0
27	0%	0
28	0%	0
29	0%	0
30	0%	0

六、对参赛者的要求

参赛者须熟悉人工智能、模拟集成电路设计,具有良好的编程能力,面向专业为:集成电路设计、计算机科学与技术、人工智能、电子科学与技术和微电子与固体电子学等。

七、参考资料

[1]. Z. Wu and I. Savidis, "Transfer Learning for Reuse of Analog Circuit Sizing Models

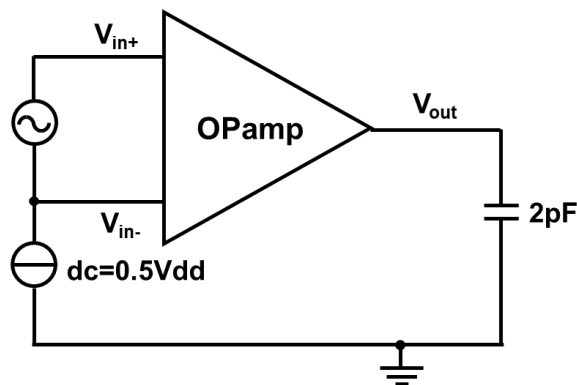
Across Technology Nodes," 2022 IEEE International Symposium on Circuits and Systems (ISCAS), Austin, TX, USA, 2022, pp. 1033-1037.

八、附录及赛题补充资料

本赛题中的运算放大器的测试电路如下：

由第一个测试电路来测量运算放大器的增益，单位增益带宽和相位裕度，并且其操作电压为 V_{dd} ，其负载电容为 2 pF ，输入共模电压为 $0.5V_{dd}$ ，扫频范围 0.1 Hz 到 100 GHz 。其中增益为频率是 1 Hz 时的增益（单位为 X ，非 dB ）。单位增益带宽（单位为 Hz ）是增益下降到 1 时的频率。相位裕度（单位为 $^\circ$ ）为增益为 1 时，相位与 -180° 的差值。

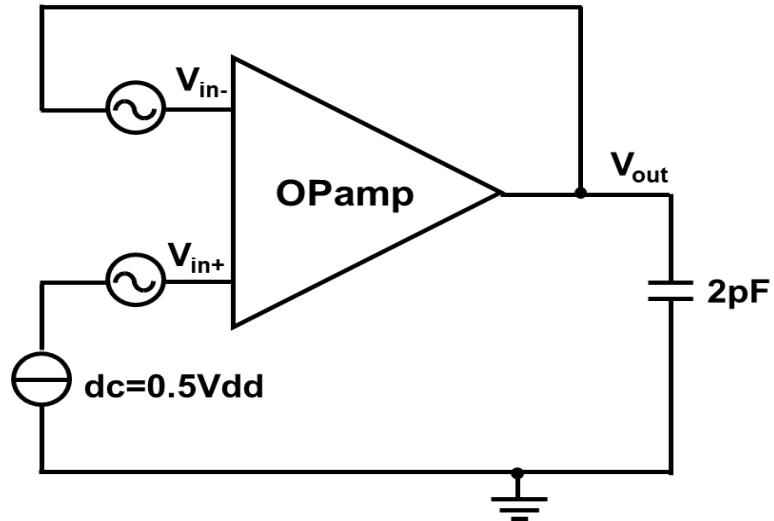
AC testbench for Gain, UGF and PM



图附 1: 测试电路 1 用于测量运算放大器的增益，单位增益带宽和相位裕度

由第二个测试电路来测量运算放大器的共模抑制比，并且其操作电压为 V_{dd} ，其负载电容为 2 pF ，输入共模电压为 $0.5V_{dd}$ ，扫频范围 0.1 Hz 到 100 GHz ，其中共模抑制比为频率是 1 Hz 时的增益（单位为 X ，非 dB ）。

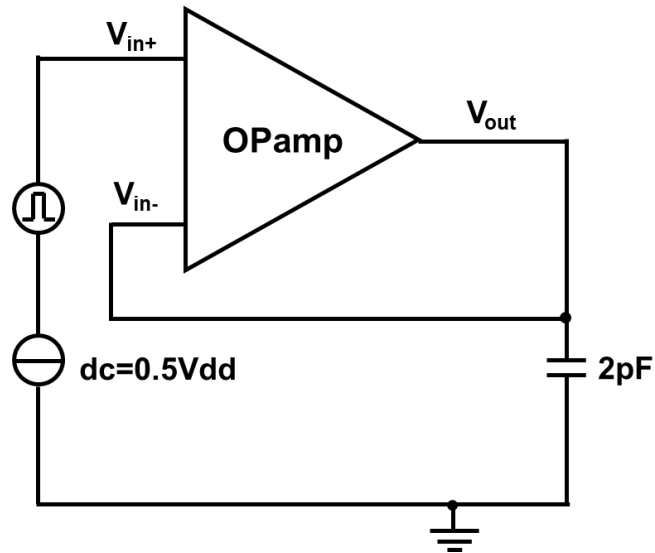
AC testbench for CMRR



图附 2: 测试电路 2 用于测量运算放大器的共模抑制比

由第三个测试电路来测量运算放大器的正向压摆率，并且其操作电压为 V_{dd} ，其负载电容为 2pF ，输入共模电压为 $0.5V_{dd}$ ，输入的正向阶跃信号的波形高度为 200mV ，上升沿 10ps ，仿真时间 100ns 。正向压摆率（单位是 V/s ）是输入阶跃信号时，输出电压正向变化的速率。

Transient testbench for SR



图附 3: 测试电路 3 用于测量运算放大器的正向压摆率

本题所用到的两个放大器，5T 运算放大器和两级运算放大器，电路网表如下

```
.subckt diff_opamp dd gnd inp inn net7 out
X1 net1 inp net3 net3 nmos W={w1} L={l1}
X2 out inn net3 net3 nmos W={w1} L={l1}
X3 net1 net1 dd dd pmos W={w2} L={l2}
X4 out net1 dd dd pmos W={w2} L={l2}
X5 net3 net7 gnd gnd nmos W={w3} L={l3}
X6 net7 net7 gnd gnd nmos W={w3} L={l3}
.ends
```

图附 4: 5T 运算放大器的电路网表

```
.subckt diff_opamp dd gnd inp inn net7 out

X1 net1 inn net3 net3 nmos W={w1} L={l1}
X2 net2 inp net3 net3 nmos W={w1} L={l1}
X3 net1 net1 dd dd pmos W={w2} L={l2}
X4 net2 net1 dd dd pmos W={w2} L={l2}
X5 net3 net7 gnd gnd nmos W={w3} L={l3}
X6 out net2 dd dd pmos W={w4} L={l4}
X7 out net7 gnd gnd nmos W={w5} L={l5}
X8 net7 net7 gnd gnd nmos W={w3} L={l3}
cc net8 out {cc}
r1 net2 net8 {cr}

.ends
```

图附 5:两级运算放大器的电路网表

*本赛题指南未尽问题，见赛题 Q&A 文件

2025 China Postgraduate IC Innovation Competition • EDA Elite Challenge Contest

1. Problem

AI-Based Cross Technology Behavioral Modeling of Analog ICs

2. Company

Hong Kong Applied Science and Technology Research Institute Company Limited

3. Problem Background

With the continuous and rapid advancement of the global integrated circuit (IC) industry, analog integrated circuits, as core building blocks of system-on-chip (SoC), are playing an increasingly vital role. A key challenge in analog IC design is how to reuse existing intellectual property (IP) blocks effectively to achieve agile design in new process nodes, thereby shortening time-to-market, which is not only a market need, but also a technical challenge. This contest problem “AI-based across-technology behavioral modeling for analog integrated circuits” is proposed based on the need and challenge. Achieving cross-technology analog IC design automation involves two aspects: automatic migration, i.e. porting (resizing) of circuit schematics and automatic migration of physical layouts. In view of the complexity of this task and the time limitation of the competition, the scope of this contest problem will be limited to cross-technology circuit modeling, which is related to the automatic migration, namely re-sizing of circuit schematics.

Currently, machine learning techniques, such as deep neural networks (DNN), Gaussian process regression (GPR), and support vector machines (SVM), have opened a new avenue

for cross-technology node modeling research because of their powerful data-driven modeling capabilities. The development of predictive model using history data in previous process nodes has emerged as a key focus in this field. Accurate cross- process node modeling enables early circuit performance evaluation during new technology introduction, significantly reducing design verification cycles. However, the critical challenge of utilizing large-scale source technology data to improve model generalization with limited target technology data still requires joint efforts from both academia and industry.

4. Competition Problem Description

This competition task focuses on predicting analog circuit performance cross process nodes. Participants are required to design new algorithms, including artificial intelligence (AI) approaches such as machine learning (ML), transfer learning (TL), and large language models (LLMs), or any other methods, using training data provided in source process A and target process B. This dataset contains abundant circuit simulation data from process A and limited data from process B, covering 2 different operational amplifier topologies, two-stage and five-transistor op-amps. A withheld test set comprises extensive Technology B simulation data. Participants will develop models using the complete training dataset and circuit topology information provided by the organizers. Final submissions will undergo rigorous assessment of accuracy and generalization performance on the hidden test set.

(Participants need to address the following challenges):

4.1 Problem Statement

Participants must develop cross-process circuit models using the provided dataset, containing abundant simulation data from source Technology A and limited data from target Technology B. These models will include: (a) predict performance metrics, as shown in Figure 1, and (b) inverse design, as shown Figure 4, of two operational amplifier topologies.

A. 5T Operational Amplifier Performance Prediction Model

The inputs of this model are circuit design parameters of a 5T operational amplifier, as shown in Figure 2, including device dimensions and bias currents, and the outputs are predicted circuit performance metrics, such as DC gain, unity-gain frequency (UGF), phase margin (PM), common-mode rejection ratio (CMRR), and slew rate (SR), under target Technology B.

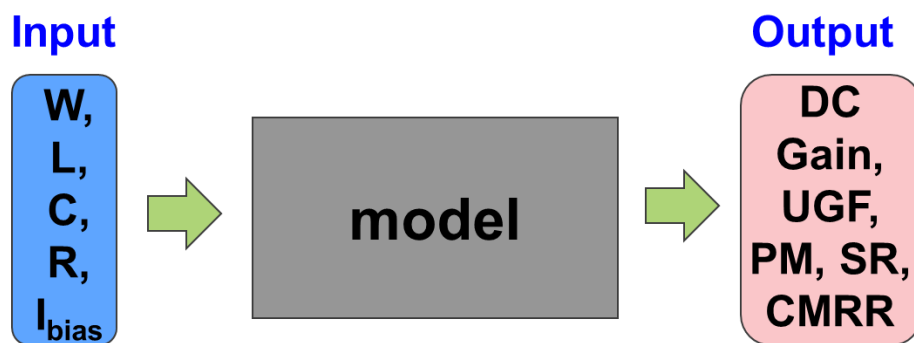


Fig. 1 Operational Amplifier Performance Prediction Model

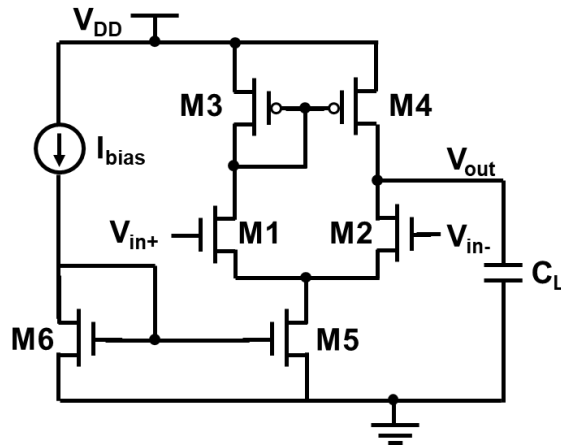


Fig.2 Circuit topology of 5T operational amplifier

Circuit design parameters	unit	Circuit performance indicators	unit
w1	um	Gain	X
w2	um	PM	°
w3	um	UGF	Hz
l1	um	CMRR	X
l2	um	SR	V/s
l3	um		
I _{bias}	A		

Table 1: Circuit design parameters and performance indicators of the 5T operational amplifier

B. wo-Stage Operational Amplifier Performance Prediction Model

The inputs of this model are design parameters of the two-stage operational amplifier, as shown in Figure 3, including device dimensions and bias currents, and the outputs are predicted circuit performance metrics, such as Gain, UGF, PM, CMRR, and SR, under target Technology B.

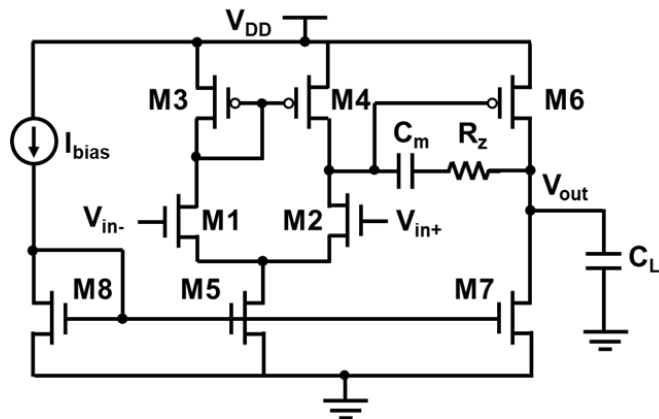


Fig. 3: Circuit topology of a two-stage operational amplifier

Circuit design parameters	unit	Circuit design parameters	unit	Circuit performance indicators	unit
w1	um	l1	um	Gain	X
w2	um	l2	um	PM	°
w3	um	l3	um	UGF	Hz
w4	um	l4	um	CMRR	X
w5	um	l5	um	SR	V/s
Cm	F	I _{bias}	A		
Rz	ohm				

Table 2: Circuit design parameters and performance indicators of a two-stage operational amplifier

C. T Operational Amplifier Parameter Inversion Model

The inputs of this model are the performance metrics of the 5T operational amplifier based on process technology B, including gain, UGF, PM, CMRR and SR, and the outputs are predicted design parameters, such as transistor dimensions and bias currents, achieving inverse circuit design under Technology B.

D. Two-stage operational amplifier parameter back-calculation model

The inputs of this model are the performance metrics of the two-stage operational amplifier based on the technology B, including gain, UGF, PM, CMRR and SR, and then the outputs are predicted design parameters, such as transistor dimensions and bias currents, achieving inverse circuit design under Technology B.

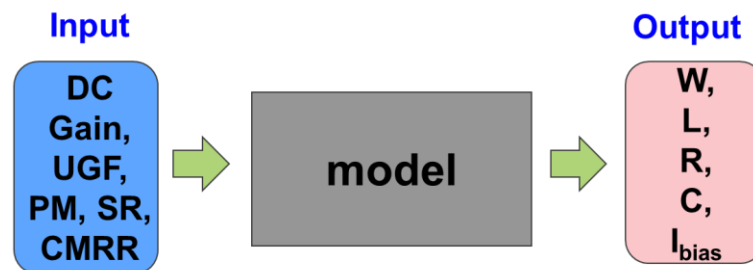


Fig. 4: Parameter Back-Calculation Model of the Operational Amplifier

4.2 Submission Requirements

Final competition submissions must include two components:

3. Source Code Repository: Submit executable algorithm code with a Python interface. The implementation must feature clear architecture, comprehensive documentation, and full reproducibility.
4. Design Report (Word Format): Submit a team technical report, including algorithm design methodology, detailed experimental test analysis and comprehensive performance summary. The report must demonstrate logical coherence and thorough technical discussion

5. Scoring Criteria

Total (Sections A, B, C, and D): 100 points, each section: 25 points. Submitted programs will be evaluated on both 5T and two-stage operational amplifiers. Ranking will be determined through comprehensive assessment of prediction accuracy and model generalization capability, with final scores assigned according to competition ranking.

Scoring criteria per section:

3. Prediction Accuracy Score (20%): Models will be evaluated on target Process B data within the training dataset. Prediction precision will be quantified using error metrics between model outputs and ground truth data, including Mean Squared Error (MSE), Mean Absolute Error (MAE), and Coefficient of Determination (R^2). The organizing committee will calculate a Figure of Merit (FoM) based on these metrics to score submissions. Teams will then be ranked according to FoM results, with higher rankings receiving proportionally greater scores.
4. Generalization Capability Score (80%): This primary evaluation focuses on model stability and adaptability when processing the withheld test dataset, specifically assessing performance under scarce target-process data conditions. The organizing committee will quantify generalization capability using error metrics between predictions and test data ground truth, including MSE, MAE, and R^2 . A FoM derived from these metrics will determine team rankings, with higher rankings receiving proportionally greater scores.

Detailed scoring methodology:

For Sections A and B, the Figure of Merit (FoMi) for the i th performance metric (or inverse design parameter) is calculated as follows:

$$FoM_i = 0.3 \times MSE_{nom} + 0.3 \times MAE_{nom} + 0.4 \times R^2_{norm} \quad (1)$$

$$MSE_{nom} = 1 - \min(MSE / MSE_{worst}, 1) \quad (2)$$

$$MAE_{nom} = 1 - \min(MAE / MAE_{worst}, 1) \quad (3)$$

$$R^2_{norm} = \max(R^2, 0) \quad (4)$$

where MSE_{worst} denotes the poorest MSE observed among all teams for the i th circuit performance metric (or inverse design parameter), and MAE_{worst} represents the highest MAE for the i th metric across all submissions.

The total FoM is:

$$FoM = \sum (FoM_i) \quad (5)$$

For Sections A and B, teams are ranked according to their FoM (Eq. 5). Score allocation follows this structure: Rank 1 has 100% of section score, Rank 2 gets 90%, Rank 3 gets 80%, Ranks 4 to 10 decreases by 5% per rank, namely from 75% to 45%, Ranks 11 to 25 decreases by 3% per rank, namely from 42% to 0%.

In Sections C and D, calculate the FoM for the inverse design parameters of the circuit:

$$FoM = 0.5 \times MSE'_{nom} + 0.5 \times MAE'_{nom} \quad (6)$$

$$MSE'_{nom} = 1 - \min(MSE' / MSE'_{worst}, 1) \quad (7)$$

$$AE'_{nom} = 1 - \min(MAE' / MAE'_{worst}, 1) \quad (8)$$

$$MSE' = \frac{1}{n} \sum_{i=1}^n \sum_{k=1}^k \left(\frac{y_k - y_k'}{y_k} \right)^2 \quad (9)$$

$$MAE' = \frac{1}{n} \sum_{i=1}^n \sum_{k=1}^k \left| \frac{y_k - y_k'}{y_k} \right| \quad (10)$$

Where MSE'_{worst} denotes the worst MSE' of the inverse design parameters among all submissions, while MAE'_{worst} represents the worst MAE' of the inverse design parameters among all submissions. Specifically, y_k stands for real value of the k th design parameter, y_k' denotes the predicted k th design parameter, and n is the number of samples.

For Sections C and D, teams are ranked according to Eq. (6).

Finally, the final ranking is determined based on the total scores of each team in the four parts A, B, C and D.

Taking the generalization score of Section A as an example, the full score for the generalization score in Section A is $25 \times 80\% = 20$ points. The following table shows the generalization scores of the top 30 participating teams in Section A:

Ranking	The relative generalization score of Part A [%]	The absolute generalization score of Part A
1	100%	20
2	90%	18
3	80%	16
4	75%	15
5	70%	14
6	65%	13
7	60%	12

8	55%	11
9	50%	10
10	45%	9
11	42%	8.4
12	39%	7.8
13	36%	7.2
14	33%	6.6
15	30%	6
16	27%	5.4
17	24%	4.8
18	21%	4.2
19	18%	3.6
20	15%	3
21	12%	2.4
22	9%	1.8
23	6%	1.2
24	3%	0.6
25	0%	0
26	0%	0
27	0%	0
28	0%	0
29	0%	0
30	0%	0

6. Requirements for participants

Participants are required to have a good command of artificial intelligence and analog integrated circuit design, as well as excellent programming skills. The major of the participants are integrated circuit design, computer science and technology, artificial intelligence, electronic science and technology, and microelectronics and solid-state electronics, etc.

7. Reference

- [1]. Z. Wu and I. Savidis, "Transfer Learning for Reuse of Analog Circuit Sizing Models

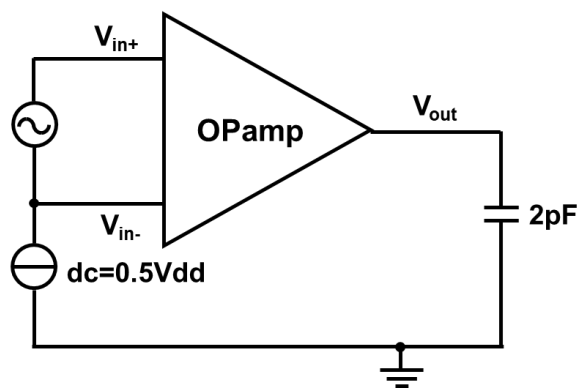
Across Technology Nodes," 2022 IEEE International Symposium on Circuits and Systems (ISCAS), Austin, TX, USA, 2022, pp. 1033-1037.

8. Appendices and Supplementary Materials

In this competition problem, the test circuit for the operational amplifier is as follows :

The first test circuit is used to measure the gain, unity-gain bandwidth, and phase margin of the operational amplifier, with an operating voltage of V_{dd} , a load capacitance of 2 pF, an input common-mode voltage of $0.5V_{dd}$, and a frequency sweep range from 0.1 Hz to 100 GHz. The gain refers to the gain at a frequency of 1 Hz (in X, not dB). The unity-gain bandwidth (in Hz) is the frequency at which the gain drops to 1. The phase margin (in degrees) is the difference between the phase and -180° when the gain is 1.

AC testbench for Gain, UGF and PM

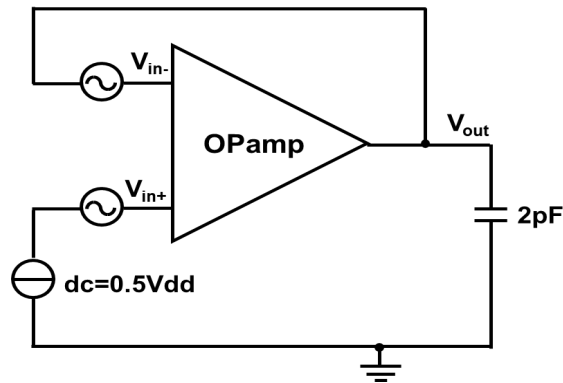


Appendix. 1: Test circuit 1 is used to measure the gain, unity gain bandwidth and phase margin of the operational amplifier.

The second test circuit is employed to measure the common-mode rejection ratio (CMRR) of the operational amplifier, with an operating voltage of V_{dd} , a load capacitance of 2 pF, an input common-mode voltage of $0.5V_{dd}$, and a frequency sweep range from 0.1

Hz to 100 GHz. Herein, the CMRR refers to the gain at a frequency of 1 Hz (in X, not dB).

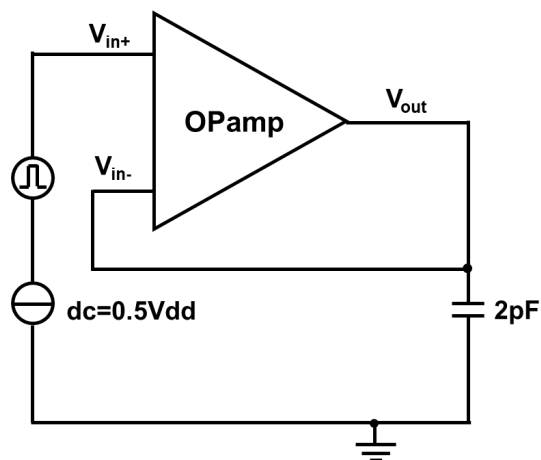
AC testbench for CMRR



App. 2: Test Circuit 2 is used to measure the common-mode rejection ratio of the operational amplifier.

The third test circuit is used to measure the positive slew rate of the operational amplifier, with an operating voltage of V_{dd} , a load capacitance of 2 pF , an input common-mode voltage of $0.5V_{dd}$. The input positive step signal has a waveform amplitude of 200 mV , a rising edge of 10 ps , and a simulation time of 100 ns . The positive slew rate (in V/s) refers to the rate of positive change in the output voltage when an input step signal is applied.

Transient testbench for SR



App. 3: Test circuit 3 is used to measure the positive slew rate of the operational amplifier.

The netlists of two operational amplifiers used in this problem, namely the 5T operational amplifier and the two-stage operational amplifier, are as follows:

```
.subckt diff_opamp dd gnd inp inn net7 out

X1 net1 inp net3 net3 nmos W={w1} L={l1}
X2 out inn net3 net3 nmos W={w1} L={l1}
X3 net1 net1 dd dd pmos W={w2} L={l2}
X4 out net1 dd dd pmos W={w2} L={l2}
X5 net3 net7 gnd gnd nmos W={w3} L={l3}
X6 net7 net7 gnd gnd nmos W={w3} L={l3}

.ends
```

App. 4: Circuit netlist of 5T operational amplifier

```
.subckt diff_opamp dd gnd inp inn net7 out

X1 net1 inn net3 net3 nmos W={w1} L={l1}
X2 net2 inp net3 net3 nmos W={w1} L={l1}
X3 net1 net1 dd dd pmos W={w2} L={l2}
X4 net2 net1 dd dd pmos W={w2} L={l2}
X5 net3 net7 gnd gnd nmos W={w3} L={l3}
X6 out net2 dd dd pmos W={w4} L={l4}
X7 out net7 gnd gnd nmos W={w5} L={l5}
X8 net7 net7 gnd gnd nmos W={w3} L={l3}
cc net8 out {cc}
r1 net2 net8 {cr}

.ends
```

App. 5: Circuit netlist of two-stage operational amplifier

*For questions not covered in this guide, please refer to the O&A document